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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,296	03/09/2004	Dana Lee	2102397-992471	4439

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,296	LEE ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the request for reconsideration filed 25 November 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (U.S. Patent 6,541,815).

Mandelman discloses a memory device (Figs. 1,2 and 16B) that contains memory cell for storage of a plurality of bits comprising a single crystalline silicon substrate (10) of first conductivity type and having planar surface, a trench in substrate, having a sidewall (18) perpendicular to the planar surface and bottom wall (20), a first region (D1/D2/Fig. 2) of second conductivity along the bottom wall of the trench, a second region (S0-2/36/Figs. 2 and 1) along the bottom wall, a channel region having a first portion (area between second regions along the sidewall) and a second portion (area along planar surface where D1-2 are located), connecting the first and second

regions for the conduction of charges, wherein the first portion is along the surface adjacent to first region and the second portion is along the sidewall adjacent the second region, a dielectric (12/28/42) on the channel region, a floating gate (30) in trench on dielectric spaced apart from the second portion, a first gate electrode (58) on the dielectric spaced apart from the first portion and second gate electrode (80) in the trench coupled to the floating gate, where the floating gate has a tip portion substantially adjacent to the gate electrode. As can be seen in Fig. 2, there is a second dielectric between floating gate (FG1A) and first gate (C1) and between floating gate (FG1A) and bottom wall of trench, which permits Fowler-Nordheim tunneling of electrons from floating gate and first gate electrode.

Claims 6-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (U.S. Patent 6,541,815).

Mandelman discloses a memory device (Fig. 16B) that contains an array of memory cells arranged in columns and rows, where each memory cell comprises a single crystalline silicon substrate (10) of first conductivity type and having planar surface, a plurality of trenches in substrate and parallel to each other, having a sidewall (18) perpendicular to the planar surface and bottom wall (20), a first region (D1/D2/Fig. 2) of second conductivity along surface, a second region (S0-2/36/Figs. 2 and 1) of second conductivity along the bottom wall of trench, a channel region having a first portion (area between second regions along the sidewall) along the sidewall of the first trench, second portion (area along planar surface where D1-2 are located) along the sidewall of the second trench, a dielectric (12/28/42) on the channel region, a floating

gate (30) on dielectric spaced apart from the second portion, a first gate electrode (58) on the dielectric spaced apart from the first portion, an second gate electrode (80) in the trench coupled to the floating gate, where the floating gate has a tip portion adjacent to the first gate electrode. In regards to the second trench, as seen in Figs.1 and 2 there are more than on trench in the memory cell and all the trenches contain the same elements as the first trench, therefore the second trench contains a second region, floating gate and control gate, where the cells in the same row have the same gate electrode and cells in the same column have the same first region, second region, control gates in common and the cell in adjacent columns have first region and first control gate in common. As can be seen in Fig. 2, there is a second dielectric between floating gate (FG1A) and first gate (C1) and between floating gate (FG1A) and bottom wall of trench, which permits Fowler-Nordheim tunneling of electrons from floating gate and first gate electrode.

Claims 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al. (U.S. Patent 6,541,815).

Mandelman discloses a memory device (Fig. 16B) that contains an array of memory cells arranged in columns and rows, where each memory cell comprises a single crystalline silicon substrate (10) of first conductivity type and having planar surface, a first trench and second trench in substrate and parallel to each other, having a sidewall (18) perpendicular to the planar surface and bottom wall (20), a first region (S0-2/36/Figs. 2 and 1) of second conductivity along the bottom wall of the trench, a floating gate (30) in the trench along the sidewall, a first gate electrode (80) in the trench

insulated from the first region and capacitively coupled to the floating gate, a second region (D1/D2/Fig. 2) of second conductivity in substrate along the surface of trench, a second gate electrode (58) spaced apart from the surface between the second region and trench. In regards to the second trench, as seen in Figs.1 and 2 there are more than on trench in the memory cell and all the trenches contain the same elements as the first trench, therefore the second trench contains a second region, floating gate and control gate, where the cells in the same row have the same gate electrode and cells in the same column have the same first region, second region, control gates in common and the cell in adjacent columns have first region and first control gate in common. As can be seen in Fig. 2, there is a second dielectric between floating gate (FG1A) and first gate (C1) and between floating gate (FG1A) and bottom wall of trench, which permits Fowler-Nordheim tunneling of electrons from floating gate and first gate electrode.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

Zandra V. Smith
Supervisory Patent Examiner
3. Feb. 2006